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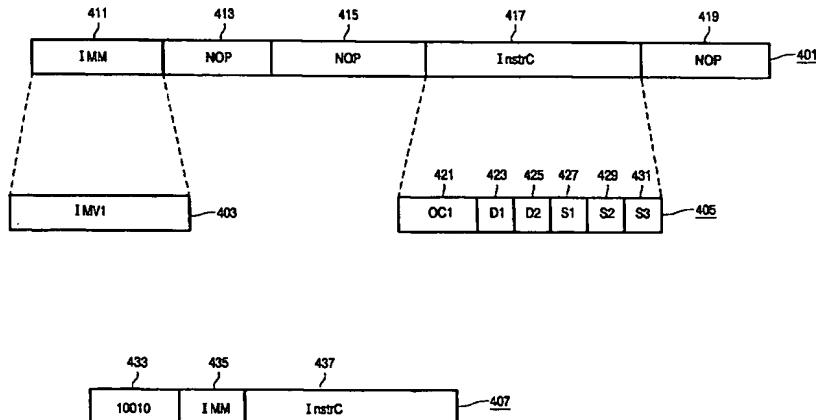
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(54) Title: APPARATUS, METHOD ,AND COMPILER ENABLING PROCESSING OF LOAD IMMEDIATE INSTRUCTIONS IN A VERY LONG INSTRUCTION WORD PROCESSOR



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(57) Abstract: Differences in encoding efficiency of instructions may arise if certain operations require very large immediate values as operands, as opposed to others requiring no immediate values or small immediate values. The present invention describes a processing apparatus, a compiler as well as a method for processing data, allowing the use of instructions that require large immediate data, while simultaneously maintaining an efficient encoding and decoding of instructions. The processing apparatus comprises a plurality of issue slots (UC0, UC1, UC2, UC3), wherein each issue slot comprises a plurality of functional units (FU20, FU21, FU22). The processing apparatus is arranged for processing data, based on control signals generated from a set of instructions being executed in parallel. The processing apparatus further comprises a dedicated issue slot (UC4) arranged for loading an immediate value (IMV1) in dependence upon a dedicated instruction (IMM). The immediate value (IMV1) can be stored in a dedicated register file (RF2) and the issue slot requiring this value can retrieve it from the dedicated register file (RF2).



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A. CLASSIFICATION OF SUBJECT MATTER  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 886 210 A (MATSUSHITA ELECTRIC IND CO LTD) 23 December 1998 (1998-12-23) the whole document ---	1-4,6-12
Y	EP 0 899 656 A (MATSUSHITA ELECTRIC IND CO LTD) 3 March 1999 (1999-03-03) the whole document ---	5
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Y	WO 98/27486 A (HEWLETT PACKARD CO) 25 June 1998 (1998-06-25) page 6, line 12 -page 8, line 21 ---	5

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Information on patent family members

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